```
     (FILE 'USPAT' ENTERED AT 19:01:49 ON 12 MAR 1999)
L1           440 S BURST (P) (PIPELIN? OR PIPE LIN####)
L2           147 S L1 (P) MODE
L3           110 S L2 (P) MEMORY
L4            29 S L3 AND FY<1995
L5             9 S L3 (P) EDO
L6            14 S L3 AND EDO
```

=> s 5392239/pn

L1 1 5392239/PN

=> s l1 and internal

539424 INTERNAL
2499 INTERNALS
540500 INTERNAL
(INTERNAL OR INTERNALS)
L2 1 L1 AND INTERNAL

=> d kwic 1-

US PAT NO: **5,392,239** [IMAGE AVAILABLE] L2: 1 of 1

DETDESC:

DETD(23)

Unlike . . . at times 91, 92, 93, 94, 95, 96, 97, are each detected by burst mode detector 16, which then sets **internal** timing for address counter 14 to increment, during each detected CAS signal 81 rising or falling edge, the stored column. . .

=> s 5610864/pn or 4851990/pn

1 5610864/PN
1 4851990/PN
L3 2 5610864/PN OR 4851990/PN

=> s l1 or l2

L4 1 L1 OR L2

=> s p4 and (pipe or pipeline or pipelined or pipelining)

10573 P4
198413 PIPE
88160 PIPES
221585 PIPE
(PIPE OR PIPES)
22406 PIPELINE
10733 PIPELINES
26434 PIPELINE
(PIPELINE OR PIPELINES)
4474 PIPELINED
2530 PIPELINING
3 PIPELININGS
2531 PIPELINING
(PIPELINING OR PIPELININGS)
L5 1146 P4 AND (PIPE OR PIPELINE OR PIPELINED OR PIPELINING)

=> s l4 and (pipe or pipeline or pipelined or pipelining)

198413 PIPE
88160 PIPES

221585 PIPE
(PIPE OR PIPES)
22406 PIPELINE
10733 PIPELINES
26434 PIPELINE
(PIPELINE OR PIPELINES)
4474 PIPELINED
2530 PIPELINING
3 PIPELININGS
2531 PIPELINING
(PIPELINING OR PIPELININGS)
L6 0 L4 AND (PIPE OR PIPELINE OR PIPELINED OR PIPELINING)

=> s (pipe or pipeline or pipelined or pipelining) and (l1 or l3)

198413 PIPE
88160 PIPES
221585 PIPE
(PIPE OR PIPES)
22406 PIPELINE
10733 PIPELINES
26434 PIPELINE
(PIPELINE OR PIPELINES)
4474 PIPELINED
2530 PIPELINING
3 PIPELININGS
2531 PIPELINING
(PIPELINING OR PIPELININGS)
L7 2 (PIPE OR PIPELINE OR PIPELINED OR PIPELINING) AND (L1 OR L3
)

L1 114 S BURST (P) (PIPELIN? OR PIPE LIN####) (P) MODE
L2 9 S EDO AND L1

1. 5,812,492, Sep. 22, 1998, Control signal generation circuit and semiconductor memory device that can correspond to high speed external clock signal; Tadaaki Yamauchi, et al., 365/233.5, 193 [IMAGE AVAILABLE]

US PAT NO: 5,812,492 [IMAGE AVAILABLE] L2: 1 of 9
DATE FILED: Jan. 10, 1997

SUMMARY:

BSUM(5)

A semiconductor device that can operate in an operation mode called **EDO** (Extended Data Output) mode or hyper page mode is known as one semiconductor memory device that operates at a high. . .

SUMMARY:

BSUM(13)

A semiconductor memory device operating in a **pipe line burst mode** (**burst EDO mode**), for example, is developed as a semiconductor memory device that has the cycle time period of data output reduced.

SUMMARY:

BSUM(14)

FIG. 24 is a timing chart showing a data read out operation of a semiconductor memory device with a **pipe line burst mode**. At time t1, row address strobe signal ZRAS attains an L level and X address signal X1 is entered. At. . .

SUMMARY:

BSUM(17)

In this **pipe line burst mode**, the data of the memory cell selected by the column address entered at time t2 should be output at the. . .

SUMMARY:

BSUM(20)

In this **pipe line burst mode**, input of another column address during data output allows memory cell data of four addresses to be selected according to. . .

SUMMARY:

BSUM(21)

This . . . at a higher rate with respect to a CPU (Central Processing Unit) which is an external processor. Similarly in this **pipe line burst mode**, data output terminal DQ attains an high impedance state when signals ZRAS and ZCAS both attain an H level to. . .

DRAWING DESC:

DRWD(25)

FIG. 24 is a timing chart showing an operation of a **pipe line burst mode** according to a conventional semiconductor memory device.

DETDESC:

DETD(28)

Signal line SIGNN is connected to an input portion of an inverter INV. An operation **mode** designating signal **/BURST** is output from inverter INV. When this operation **mode** designating signal **/BURST** attains an H level, a readout operation of **mode** 1 (for example, a high speed page **mode**) is designated. When operation **mode** designating signal **/BURST** is set to an L level, a readout operation of **mode** 2 (for example, a **pipe line burst mode** 2) is specified.

2. 5,812,470, Sep. 22, 1998, Apparatus, system and method for identifying semiconductor memory access modes; Roland Ochoa, et al., 365/201, 225.7, 230.08, 238.5 [IMAGE AVAILABLE]

US PAT NO: 5,812,470 [IMAGE AVAILABLE] L2: 2 of 9
DATE FILED: Sep. 10, 1996

SUMMARY:

BSUM(5)

Semiconductor . . . as DRAMs can function in a number of operational modes. These modes include fast page mode (FPM), extended data out (**EDO**) mode, and burst extended data out (BEDO). Typically, the DRAM includes separate circuit blocks corresponding to each of these operational. . .

DETDESC:

DETD(7)

Extended Data-out Mode (**EDO**) is similar to FPM, except that CAS# going HIGH does not disable the data outputs. Instead, a data latch is. . .

DETDESC:

DETD(8)

Burst Extended Data-out **Mode** (BEDO) differs from **EDO** in two ways. First, because the data latch is replaced by a register (i.e., an additional latch stage is added), data will not reach an output as a result of a first CAS# cycle. The benefit of this internal **pipeline** stage is that data will appear in a shorter time from the activating CAS# signal edge in the second CAS#. . . CAC (maximum access time from CAS# HIGH-to-LOW transition) is shorter. The second difference is that the access circuits for this **mode** include an internal address counter so that only the initial address in a **burst** of four needs to be provided externally. Moreover, there is in fact no additional delay in receiving the first data. .

DETDESC:

DETD(9)

In . . . I/O buffers and array 17 in array control block 18. Similar

fuses 14B and 14C to selectively power up the **EDO** and fast page mode (FPM) circuit blocks 16B and 16C, respectively, are supplied via similar control paths (including, for example,. . .

DETDESC:

DETD(16)

Similar operations occur in circuits 11B and 12B, or 11C and 12C, if **EDO** or FPM are selected.

3. 5,805,873, Sep. 8, 1998, Phase linking of output clock with master clock in memory architecture; Richard Stephen Roy, 395/557, 559 [IMAGE AVAILABLE]

US PAT NO: 5,805,873 [IMAGE AVAILABLE] L2: 3 of 9
DATE FILED: May 20, 1996

SUMMARY:

BSUM(19)

A . . . utilize a pipelined structure, as in the synchronous SRAMs mentioned previously. Other examples of pipelined structures include Extended Data Out (**EDO**) DRAMs, synchronous DRAMs, and RAMBUS.TM. DRAMs (or RDRAMS).

SUMMARY:

BSUM(20)

The most evolutionary modification to the standard DRAM architecture is the advent of the **EDO** DRAMs. This is a relatively minor modification to the column mode circuitry of the DRAM which allows a faster usable. . . and column access times are unchanged from the standard DRAM architecture. A further enhancement of this technique is a Burst **EDO**, in which a burst counter is added to the DRAM to allow sequential data bytes stored within the device to. . . be accessed without having to supply new addresses for each data byte. Instead, the burst counter supplies the addresses. These **EDO** DRAM architectures are expected to achieve data bandwidth rates in the 132 MB/sec range for sixteen-bit devices in the near. . .

SUMMARY:

BSUM(21)

A more sophisticated evolutionary approach to achieving higher **pipelined** bandwidth is the synchronous DRAM, in which a master clock signal and other architectural enhancements provide faster usable **burst** cycle times than either **EDO** or **Burst EDO** DRAMs. In synchronous DRAMs, data available on column sense amplifiers following a row access is used to create a **burst mode**, which can reduce cycle time to the 10 ns range. Subsequent data can be streamed out from the column sense amplifiers at 10 ns intervals due to the **pipeline** configuration, which results in a 100 MHz data rate. Synchronous DRAMs have a random access time of about 60 ns,. . .

DETDESC:

DETD(105)

Within the central bank control logic unit 36, there is an additional counter that is loaded with the transaction **burst** length and keeps track of how many **burst** cycles remain to complete the transaction. This **burst** length counter (as opposed to the **burst** counter

coupled to the column address buffers) allows the data to keep flowing until the desired **burst** length is reached. When the end of a **burst** is reached, the **burst** length counter produces a flag signal, which can be used to initiate the transaction from the next-up register 56, if. . . the current transaction. It may be possible to re-use the same counter circuit to implement the same function for the **pipelined** random column **mode**, with minor modification.

DETDESC:

DETD(110)

The **pipelined** random column access **mode** contrasts with normal row or column **burst** accesses which only provide sequential or interleaved internal addresses for each consecutive operation from the **burst** counter. Instead, a new column address can be provided across interface 1 every cycle for a **pipelined** random read operation, which can be located anywhere on the selected row. Data from each new random column address is. . . cycle, with alternating data and column address information provided in a unique packet format. Thus, the transaction frequency of a **pipelined** random column write access is one-half the frequency of either a **pipelined** random column read access or conventional column **burst** transaction. It is also possible to define the random column write **mode** to send two or more bytes of data for each new byte-wide column address.

DETDESC:

DETD(112)

Referring . . . FIGS. 8 through 12, exemplary header formats for various types of read and write transactions are illustrated, including a row **burst** access (FIG. 8), a background row change (FIG. 9), a column **burst** access (FIG. 10), a **pipelined** random column **mode** (FIG. 11), and a pair of **pipelined** random column write address/data packets (FIG. 12). Each of the exemplary header formats include a plurality of nine bit words. . .

DETDESC:

DETD(132)

Another type of operation that is optimally supported by the **pipelined**, flow-through architecture of the present invention is referred to as the **pipelined** random-column read or write **mode**. In this **mode**, a new column address located anywhere within a selected row is provided across interface 1 for each byte or number of bytes that is read or written within the transaction. This contrasts with a typical column **burst** transaction, in which new column addresses are provided either sequentially or in interleaved form from the **burst** counter within the column select unit 37, starting with an initial address provided in the header.

DETDESC:

DETD(134)

The . . . a two-bit DATA.sub.-- CHANNEL[0:1] field and a one-bit COLUMN(MSB) field. The TRANS.sub.-- LENGTH[0:3] field is similar in encoding to the **BURST**.sub.-- LENGTH[0:3] field described above; however the TRANS.sub.-- LENGTH[0:3] specifies how many subsequent column address bytes will be provided across the. . . channel within the transaction. The PRECHARGE and R/W fields have the same meaning as described above with respect to column **burst** access transactions. The DATA.sub.-- CHANNEL[0:1] is also the same as described above, though it has greater importance in supporting the **pipelined** random column read

mode. The DATA.sub.--CHANNEL[0:1] field is necessary to specify an alternative target channel for providing data of a **pipelined** random read transaction, since the header channel is busy providing the new column addresses at the maximum data frequency. In a conventional column **burst** transaction, the column addresses are provided by the **burst** counter, so the header channel is free to provide the read data. Finally, the COLUMN(MSB) field specifies the most significant bit of a column address, and allows this **mode** to support column addresses that are too large by one bit to address within a single header word. The read. . .

DETDESC:

DETD(151)

FIG. 20 illustrates the **pipelined** random column read **mode** made possible by the present application. In addition to the capability of supplying a new address every cycle from an on-chip column **burst** counter, it is possible with the **pipelined** structure of the present application to provide a new random column address from the master device on every cycle of. . . possible for the column select decoding circuitry to take each new address from the input bus rather than from the **burst** counter, and at the same frequency. This **mode** is entered by use of a unique two-word header, which indicates the entry into this special **mode**. This two-word header also contains the address of the target bank, the target port (for a read), and the number of cycles to be executed within this **mode**. The row must already have been selected within the target bank before entry into this **mode**, which may be accomplished with either a background row activation transaction, or a row read or write transaction that leaves. . .

DETDESC:

DETD(152)

This **pipelined** random column read **mode** is a type of cooperative transaction in the sense that the addresses are provided on one port while the data. . . output on a different port. This is necessary since more than a small number of consecutive addresses provided in this **mode** would conflict with data coming back on the same channel. In this **mode**, the clock frequency of the output data is matched to the clock frequency of the input addresses on the input port. This contrasts with the normal cooperative **burst** clocking scheme in which CLKOUT for the read data synchronization is derived from the CLKIN supplied to the target port.. . .

DETDESC:

DETD(154)

The write version of this **pipelined** random column **mode** has some significant differences from the read version. As in the **burst** write **mode**, the write data follows the address inputs immediately on the same channel for ease of synchronization. The three preferred implementations. . .

4. 5,768,624, Jun. 16, 1998, Method and apparatus for employing ping-pong buffering with one level deep buffers for fast DRAM access; Subir K. Ghosh, 395/873; 711/157 [IMAGE AVAILABLE]

US PAT NO: 5,768,624 [IMAGE AVAILABLE] L2: 4 of 9
DATE FILED: Feb. 28, 1996

SUMMARY:

BSUM(10)

For . . . demands [redacted] the memory access circuitry. [redacted] example, one recently evolved DRAM architecture is known as the extended data out (**EDO**) standard architecture. For an example of an **EDO** DRAM, refer to the Micron Technology, Inc. data sheet entitled MT4C4007J(S) 1 Meg.times.4 DRAM which is incorporated herein by reference. The **EDO** DRAM standard allows a memory controller to shorten the pulse width of the column address strobe (CAS#) signals to the. . . DRAMs. Thus, for example, in a system operating at a host bus clock frequency of 66 MHz, a "fast page **mode**" DRAM might require CAS# to be asserted for a minimum of two clock cycles and negated for a minimum of one clock cycle, for a total access time of three clock cycles per data transfer in a **pipelined burst**. (Such memory access timing is described by the shorthand notation "X-3-3-3" for a 4-transfer sequence, where the "X" indicates an unspecified delay for the first transfer of the **burst** and each of the "3"'s indicate a 3-clock cycle delay for each of the second, third and fourth transfers of the **burst**.) An **EDO** DRAM, on the other hand, might allow CAS# to be asserted for only one clock cycle, for a total access time of only two clock cycles per data transfer in the **pipelined burst** (X-2-2-2).

SUMMARY:

BSUM(11)

The higher bandwidth transfers offered by **EDO** DRAM typically require increased buffering capacity in the buffer chips that buffer data transfers between the DRAM and host buses. . . .

DETDESC:

DETD(29)

The . . . output data is valid at its data port beginning some period of time after CAS# is asserted. For 60 nanosecond **EDO** DRAM, this delay is approximately 18 nanoseconds. Thus it can be seen from waveform 410 that eight quadwords of data, . . .

DETDESC:

DETD(36)

Thus, FIG. 4 illustrates how an 8-2-2-2 . . . host memory read access can be successfully implemented with **EDO** DRAM. The same architecture can also be used to achieve 7-2-2-2 . . . , or even 6-2-2-2, memory read. . .

DETDESC:

DETD(58)

It should be noted that whereas the timing diagram of FIG. 9 assumes that DRAM 16 is **EDO** DRAM (as can be seen by observing that MD remains valid until after the next CAS# falling edge), X-1-1-1 timing. . .

5. 5,748,914, May 5, 1998, Protocol for communication with dynamic memory; Richard Maurice Barth, et al., 395/285, 287 [IMAGE AVAILABLE]

US PAT NO: 5,748,914 [IMAGE AVAILABLE] L2: 5 of 9
DATE FILED: Oct. 19, 1995

SUMMARY:

BSUM(10)

The prior art includes Extended Data-Out (**EDO**) memory systems. In

EDO DRAMs, the output buffer is controlled by signals applied to output enable (OE) and column address stobe (CAS) control lines. In general, data remains valid at the output of an **EDO** DRAM longer than it does for conventional DRAMs. Because the data remains valid longer, the transfer of the data to. . .

SUMMARY:

BSUM(12)

The . . . clock is used to synchronize the flow of addresses, data, and control on and off the DRAM, and to facilitate **pipelining** of operations. All address, data and control inputs are latched on the rising edge of the clock. Outputs change after the rising edge of the clock. SDRAMs typically contain a **mode** register. The **mode** register may be loaded with values which control certain operational parameters. For example, the **mode** register may contain a **burst** length value, a **burst** type value, and a latency **mode** value. The **burst** length value determines the length of the data **bursts** that the DRAM will perform. The **burst** type value determines the ordering of the data sent in the **bursts**. Typical **burst** orders include sequential and sub-block ordered. The latency **mode** value determines the number of clock cycles between a column address and the data appearing on the data bus. The. . . . interval depends largely on the operating frequency of the SDRAM. Since the SDRAM cannot detect the operating frequency, the latency **mode** value is programmable by a user.

DETDESC:

DETD(22)

In typical **EDO** and SDRAM components, only a finite number of data transfer sizes are supported. For each data transfer size, there is. .

6. 5,703,829, Dec. 30, 1997, Synchronous type semiconductor memory device which can be adapted to high frequency system clock signal; Tomio Suzuki, et al., 365/233, 189.05, 230.08, 239 [IMAGE AVAILABLE]

US PAT NO: 5,703,829 [IMAGE AVAILABLE] L2: 6 of 9
DATE FILED: Jul. 23, 1996

ABSTRACT:
In a **pipeline burst EDO** operation, a latency circuit 215 detects change of an internal column address strobe signal ZCASF from an active state to. . . a non-active sate in the first cycle, and brings a signal OEMB into an active state. When a writing operation **mode** is specified, and an internal output enable signal ZOEF is in an active state, an output buffer control signal OEM. . .

SUMMARY:

BSUM(5)

Although a so-called nibble **mode**, a hyper page **mode** and the like are known as an operation **mode** of a high speed semiconductor memory device, a **pipeline burst mode** is known as an operation **mode** enabling a data reading operation at a higher speed.

SUMMARY:

BSUM(6)

FIG. 21 is a timing chart showing a data reading operation of a semiconductor memory device having this **pipeline burst mode**.

Referring to FIG. 21, the data reading operation in the **pipeline burst mode** will be described hereinafter.

SUMMARY:

BSUM(8)

In this **pipeline burst mode**, data of memory cells selected by a column address input at time t2 may be provided from the next EXT./CAS. . .

SUMMARY:

BSUM(9)

In this **pipeline burst mode**, if another column address is input during output of data, memory cell data of four addresses are selected according to. . .

DRAWING DESC:

DRWD(8)

FIG. 6 is a timing chart showing reading operation in a **pipeline burst EDO** (Extended Data Output) **mode** of the semiconductor memory device according to the first embodiment.

DRAWING DESC:

DRWD(12)

FIG. 10 is a first timing chart showing reading operation in the **pipeline burst EDO mode** of the semiconductor memory device according to the second embodiment.

DRAWING DESC:

DRWD(22)

FIG. 20 is a timing chart showing reading operation in the **pipeline burst EDO mode** of a semiconductor memory device according to a third embodiment.

DRAWING DESC:

DRWD(23)

FIG. 21 is a timing chart showing reading operation in the **pipeline burst EDO mode** of a conventional semiconductor memory device.

DETDESC:

DETD(39)

Only after detecting in a **pipeline burst EDO mode** the second change of signal ZCASF to an active state, that is, change of signal ZCASF from the H level. . .

DETDESC:

DETD(40)

On . . . brought into an active state in response to the first change of signal ZCASF to a non-active state in the **pipeline burst EDO mode**, that is, change from the L level to the H level at time t5 in FIG. 5. Therefore, it is. . .

DETDESC:

DETD(41)

FIG. . . . which should be compared to the timing chart of the conventional semiconductor memory device shown in FIG. 22 in the **pipeline burst EDO mode**.

DETDESC:

DETD(83)

FIG. 10 is a timing chart showing reading operation in the **pipeline burst EDO mode** of the semiconductor memory device shown in FIG. 9.

DETDESC:

DETD(88)

At this time, in an ordinary **pipeline burst EDO mode** operation, output buffer control signal OEM is brought into an active state in response to the activation edge of signal. . . .

DETDESC:

DETD(91)

FIG. 11 is a timing chart showing reading operation in the **pipeline burst EDO mode** in the case where the external clock signal changes at a higher speed, and where the time required for the. . .

DETDESC:

DETD(111)

The . . . not only in reading operation but also in data writing operation of a semiconductor memory device which operates in the **pipeline burst EDO mode**.

DETDESC:

DETD(112)

FIG. 15 is a timing chart showing data writing operation of the semiconductor memory device which can operate in the **pipeline burst EDO mode**.

DETDESC:

DETD(132)

FIG. 20 is a timing chart showing reading operation in the **pipeline burst EDO mode** of a semiconductor memory device including both a reading operation control circuit (output buffer control circuit 216) in the **pipeline burst EDO mode** shown in the first embodiment and internal clock generating circuit 900 shown in the second embodiment.

7. 5,692,165, Nov. 25, 1997, Memory controller with low skew control signal; Joseph M. Jeddeloh, et al., 395/551, 552; 711/100 [IMAGE AVAILABLE]

US PAT NO: 5,692,165 [IMAGE AVAILABLE] L2: 7 of 9
DATE FILED: Sep. 12, 1995

SUMMARY:

BSUM(12)

In . . . skew in applications which utilize memory devices having enhanced memory transfer modes such as page mode and extended data out (**EDO**) mode, where memory addresses located within the same page or column of a memory device may be transferred without having. . .

SUMMARY:

BSUM(16)

The invention has unique applicability with memory devices having enhanced memory transfer modes such as the **EDO** and page modes provided on many commercially available memory devices, as well as in higher speed memory devices, since in. . .

DETDESC:

DETD(16)

Preferred . . . the following U.S. patent applications, all assigned to Micron Technologies, Inc.: Ser. No. 08/370,761 filed Dec. 23, 1994 and entitled "**Burst EDO** Memory Device"; Ser. No. 08/386,894 filed Feb. 10, 1995 and entitled "**Burst EDO** Memory Device with Maximized Write Cycle Timing"; Ser. No. 08/386,563 filed Feb. 10, 1995 and entitled "**Burst EDO** Memory Device Having **Pipelined** Output"; and Ser. No. 08/455,095 filed May 31, 1995 and entitled "**Burst Mode** Block Write". The disclosures of all of these applications are hereby incorporated by reference herein. However, it will be appreciated that other random access memories such as DRAMs and other SRAMs, particularly those with enhanced data transfer **modes**, may also be used.

8. 5,668,774, Sep. 16, 1997, Dynamic semiconductor memory device having fast operation mode and operating with low current consumption; Kiyohiro Furutani, 365/233, 233.5 [IMAGE AVAILABLE]

US PAT NO: 5,668,774 [IMAGE AVAILABLE] L2: 8 of 9
DATE FILED: May 21, 1996

SUMMARY:

BSUM(11)

In . . . data is increased is proposed, for example, in Japanese Patent Laying-Open No. 59-1100945 (1984). This operation mode is called an **EDO** (Extended Data Output) mode or a hyperpage mode.

SUMMARY:

BSUM(15)

As . . . having the cycle time in the data output operation reduced, there has been disclosed a semiconductor memory device with a **pipeline burst mode** (**burst EDO mode**) shown, e.g., in "NIKKEI BYTE", April 1995, p. 142.

SUMMARY:

BSUM(16)

FIG. 52 is a timing chart representing an operation during data reading of a semiconductor memory device with the **pipeline burst**

mode. More specifically, FIG. 52 is a timing chart representing data reading operation. Referring to FIG. 52, the data read operation in the **pipeline burst mode** will now be described below.

SUMMARY:

BSUM(18)

In this **pipeline burst mode**, data of the memory cell, which is selected by the column address input at time t2, can be output in. . . can be output during the cycle period of clock signal CLOCK, and thus data can be read fast. In this **pipeline burst mode**, when another column address is input while data is being output, memory cell data at four addresses are selected in. . . data can be transferred fast to a CPU (Central Processing Unit) which is an external processing unit. Also in this **pipeline burst mode**, data output terminal DQ is set to the high impedance state when data reading is completed in response to setting. . .

SUMMARY:

BSUM(23)

In . . . signal ZRAS attains the high level at time t7 as shown in FIG. 52. This causes a problem that the **pipeline burst mode** cannot reduce time tRC.

SUMMARY:

BSUM(25)

In the structure for performing the operation in the **pipeline burst mode**, read amplifiers RAP0-RAP3 contains registers for storing the amplified data. Read amplifiers RAP0-RAP3 are provided corresponding to memory cell data. . .

SUMMARY:

BSUM(44)

Selector . . . for selecting a memory cell of 1 bit from memory cells M0-M3 of 4 bits. A DRAM operable in a **pipeline burst mode** can be easily accomplished by employing a structure which can sequentially select the memory cells to be selected simultaneously in the above test **mode**. In a 16-Mbit DRAM with the **pipeline burst mode**, therefore, a counter CNTR receives column address bits CA<1:0> and column address strobe signal ZCAS, and generates a select signal. . .

SUMMARY:

BSUM(50)

When the **pipeline burst mode** is to be implemented in the semiconductor memory device having the above structure, the counter is constructed such that a. . . accordance with column address bits CA<10:9>. According to this structure, a semiconductor memory device potentially operable in the fast page **mode** and **pipeline burst mode** is formed on the same semiconductor chip, and the structure operating in only one of these **modes** can be easily completed by a **mode** selection circuit.

DRAWING DESC:

DRWD(51)

FIG. 52 is a timing chart representing a **pipeline burst mode**

operation of the conventional semiconductor memory device;

DETDESC:

DETD(23)

The semiconductor memory device of the embodiment described above can potentially accomplish two operation **modes**, i.e., operation **mode** in which the data output terminal does not attain the high impedance state even when column address strobe signal ZCAS attains the high level of the active state, and an operation **mode** in which the data output terminal attains the high impedance state when column address strobe signal ZCAS attains the high level. Selection of these operation **modes** may be accomplished by a **mode** selection circuit or mask interconnections. As typical examples of the two operations, description will now be given on the **pipeline burst mode** and the fast page **mode**.

DETDESC:

DETD(24)

FIG. 4 shows a structure of a portion for generating a signal designating the operation **mode**. In FIG. 4, a signal line SIGLN is connected to a bonding pad BPAD, and is coupled to power supply. . . of a high resistance. Signal line SIGLN is coupled to an input of an inverter INV, from which an operation **mode** designating signal FP is output. When operation **mode** designating signal FP is at the high level, the fast page **mode** is designated. When the operation **mode** designating signal FP is at the low level, the **pipeline burst mode** is achieved. Setting of the potential level of signal FP is made a bonding wire BDWIR between bonding pad BPAD. . . fixed at the low level, and inverter INV sets signal FP to the high level, so that the fast page **mode** is designated. If bonding wire BDWIR does not exist, signal line SIGLN is set to the high level by high resistance resistor element RSTOR. In this case, signal FP attains the low level, and thus designates the **pipeline burst mode**.

DETDESC:

DETD(27)

Inhibiting gate IHGT transmits the data latched by latch circuit RLACH to read gate REGTEb when operation **mode** designating signal FP is at the high level designating the fast page **mode**. When the operation **mode** designating signal FP is at the low level designating the **pipeline burst mode**, inhibiting gate IHGT inhibits transfer of data from latch circuit RLACH to read gate REGTEb, and fixes the data signal. . .

DETDESC:

DETD(30)

When the fast page **mode** is designated (i.e., when signal FP is at the high level), data are transferred to the output buffer circuit via read gates REGTEa and REGTEb and two read data bus lines ZRBUS and RBUS. In this fast page **mode**, when column address strobe signal ZCAS attains the high level, the data output terminal attains the high impedance state. In. . . long cycle time) even if the two read data bus lines are used for charging/discharging their parasitic capacitances. In the **pipeline burst mode**, the data output terminal does not attain the high impedance state even when column address strobe signal ZCAS is set. . .

DETDESC:

DETD(31)

By . . . implement a semiconductor memory device which can operate fast with a low current consumption in any of the fast page **mode** and the **pipeline burst mode**. By selecting the bus structure in accordance with the operation **mode**, it is possible to implement a semiconductor memory device which can selectively accomplish two different **modes** on one semiconductor chip, so that the manufacturing cost can be reduced as compared with the structure where they are. . .

DETDESC:

DETD(36)

Read . . . latch instruction signal ZRDL, which will be described later in more detail, is fixed at the low level in the **pipeline burst mode** operation, and is set to and maintained at the high level for a predetermined time period in response to change of the column address signal in the fast page **mode** operation. Thus, in the **pipeline burst mode**, the output signal from NAND gate 508 is fixed at the high level, and NAND gate 509 passes the data signal sent from NAND gate 506 forming the latch (in the **pipeline burst mode**, signal FP is set to the low level). In the fast page **mode**, read data latch instruction signal ZRDL is set to the high level when reading data. In this case, NAND gate. . .

DETDESC:

DETD(39)

In the **pipeline burst mode**, signal FP is at the low level, and the output signal of NAND gate 510 is fixed at the high. . . is charged or discharged by MOS transistors 540 and 549 in accordance with the read memory cell data. In the **pipeline burst mode**, therefore, data is transferred to I/O buffer circuit only with one read data bus line ZRBUS.

DETDESC:

DETD(43)

Thereby, . . . internal data I/O lines I/Oa and ZI/O0a are transmitted onto read data bus lines RBUS0 and ZRBUS0, respectively. In the **pipeline burst mode**, such an operation is merely performed that the data signal is transmitted onto read data bus line ZRBUS0. The above. . .

DETDESC:

DETD(61)

When operation **mode** designating signal FP is at the low level and thus designates the **pipeline burst mode** operation, composite logic gate 535 inhibits passage of the signal potential on read data bus line RBUS0, and inverts and. . . the signal potential on read data bus line ZRBUS0 and transmits the same to data I/O terminal DQ. When operation **mode** designating signal FP is at the high level and thus designates the fast page **mode**, the composite logic gate 535 inhibits pass of the signal potential on read data bus line ZRBUS0, and passes the. . .

DETDESC:

DETD(63)

Output . . . described later in detail, is deactivated in response to deactivation of column address strobe signal ZCAS in the fast page **mode**. In the **pipeline burst mode**, when output buffer activating signal ZOEM is once activated, it will maintain the active state until both signals ZRAS and. . .

DETDESC:

DETD(70)

When operation **mode** designating signal FP is at the low level designating the **pipeline burst mode** as shown in FIG. 11B, externally applied column address bits A<9:2> are taken in at every fourth CAS cycle. More. . .

DETDESC:

DETD(73)

As . . . activated to attain the high level in response to falling of column address strobe signal ZCAS in the fast page **mode**. In the **pipeline burst mode**, control signal .phi.ca is activated at every fourth cycle of column address strobe signal ZCAS. A control signal .phi.cc is. . . high level in response to rising (activation) of column address strobe signal ZCAS during the remaining three cycles in the **pipeline burst mode**. Control signal .phi.cc is always inactive and at the low level in the fast page **mode**.

DETDESC:

DETD(78)

Referring to a signal waveform diagram of FIG. 13, operation in the **pipeline burst mode** will be described below. In the **pipeline burst mode**, operation **mode** designating signal FP is set to the low level. In this state, composite logic gates 740 and 741 transmit column. . .

DETDESC:

DETD(96)

When operation **mode** designating signal FP is fixed at the low level indicating the **pipeline burst mode**, the output signal of NAND gate 830 is fixed at the high level, and the output signal of NOR gate. . .

DETDESC:

DETD(99)

During . . . activated again. By utilizing the structure shown in FIG. 17, the structure operating in such a manner that, in the **pipeline burst mode**, control signal .phi.ca is active in the first ZCAS cycle, and control signal .phi.cc is active during subsequent three cycles. . .

DETDESC:

DETD(114)

When operation **mode** designating signal FP is set to the low level as shown in FIG. 22, inverter 906 turns on MOS transistor 953. It is in the **pipeline burst mode** that signal FP is set to the low level, and, in this state, counts ZCY<0> and ZCY<1> are reset to. . .

DETDESC:

DETD(116)

In the **pipeline burst mode**, data are read simultaneously from memory cells of 4 bits, and are successively selected in accordance with the addresses issued. . .

DETDESC:

DETD(144)

Referring to FIG. 29, operation in the **pipeline burst mode** will be described below. In the **pipeline burst mode**, operation **mode** designating signal FP is set to the low level, and signal ZFP is set to the high level. In this. . .

DETDESC:

DETD(155)

In the **pipeline burst mode**, the above structures operate to maintain column decoder enable signal CDE at the active state of the high level until. . . completed. Thereby, data can be successively written into the simultaneously selected memory cells of 4 bits. In the fast page **mode**, the column address is externally specified at each cycle (i.e., cycle of signal ZCAS). Therefore, by executing set/reset of the. . .

DETDESC:

DETD(159)

In the **pipeline burst mode**, as shown in FIG. 32B, operation **mode** designating signal FP is set to the low level. In this state, the output signal of inverter 913 attains the.

DETDESC:

DETD(169)

Referring first to FIGS. 34 and 35, description will be given on the operation in the **pipeline burst mode** in which operation **mode** designating signal FP is set to the low level.

DETDESC:

DETD(180)

In this operation **mode**, signal FP is fixed at the low level, and read data bus line RBUS0 is not charged/discharged. In the **pipeline burst mode** in which operation **mode** designating signal FP is set to the low level, data of 4 bits selected by the column select line are successively read. In contrast to the conventional nibble **mode**, the read amplifiers are successively activated in accordance with the order of data to be read successively, and the read. . .

DETDESC:

DETD(187)

When . . . via the I/O buffer circuit. At times t6 and t7, signals ZCAS and ZRAS are deactivated. In the fast page **mode**, false data is not output, because data reading is performed with the complementary read data bus lines, so that data can be read fast. Since the cycle time is longer than that in the **burst pipeline mode**, so that the average current consumption can be reduced.

DETDESC:

DETD(192)

This . . . both signals ZRAS and ZCAS attain the high level in FIG. 39. Thus, the semiconductor memory device operates in the **pipeline burst mode**.

DETDESC:

DETD(196)

In the **pipeline burst mode**, therefore, when memory cell data of 4 bits are simultaneously selected, last data Dd, i.e., data of fourth bit can. . .

DETDESC:

DETD(199)

Second . . . 102 receiving write enable signal ZWE, and a composite logic gate 134 receiving the output signal of inverter 102, operation **mode** designating signal FP, delayed row address strobe signal ZRASD from delay stage 2010 and externally applied column address strobe signal. . . gate 134 is equivalent to a structure which includes an OR gate receiving the output signal of inverter 102, operation **mode** designating signal FP and delayed row address strobe signal ZRASD, and an NAND gate receiving the output signal of this. . . address strobe signal ZCAS and delayed row address strobe signal ZRASD attain the high level during data reading in the **pipeline burst mode**.

DETDESC:

DETD(213)

With reference to FIG. 42, description will be given on data read operation in the **pipeline burst mode** during which operation **mode** designating signal FP is set to the low level.

DETDESC:

DETD(218)

At . . . high level. When column address strobe signal ZCAS rises to the high level at time t8, the operation in the **pipeline burst mode** is performed as already described. More specifically, the internal column address is defined, column selection is carried out, and data. . .

DETDESC:

DETD(222)

In the **pipeline burst mode**, the read **mode** signal READ is obtained by inverting the output signal of NAND gate 126. When the potential on node N4a is. . . strobe signal ZCAS attains the high level, the output signal of NAND gate 126 attains the low level, and read **mode** designating signal READ attains the high level. Thus, in the data read **mode**, when column address strobe signal ZCAS is at the high level, read **mode** designating signal READ is at the high level during a period in which data is actually and internally read, and. . .

DETDESC:

DETD(225)

FIG. 43 is a sequence chart showing the whole operation of the semiconductor memory device in the **pipeline burst mode**. At time t1, row address strobe signal ZRAS is set to the active state of the low level, and the. . .

DETDESC:

DETD(232)

At . . . for row address strobe signal ZRAS is equal to eight clock cycles, and the access to another row in the **pipeline burst mode** can be advanced by one clock cycle, compared with the conventional structure.

DETDESC:

DETD(236)

As . . . specifies a memory cell among the simultaneously selected memory cells with least significant column address bits CA<1:0>. In the test **mode**, all column address bits CA<1:0> and ZCA<1:0> (referred to as "degenerated address") are set into a selected state. Accordingly, it is possible to accomplish the semiconductor memory device which is operable in either of the fast page **mode** and the **pipeline burst mode** on the same semiconductor chip.

DETDESC:

DETD(237)

FIG. . . . used in the semiconductor memory device of 16 Mbits is used, as is, in the semiconductor memory device performing the **pipeline burst mode** operation, so that addresses are allocated as described below. Y-decoder 203 is supplied with column address bits CA<10:2>. X-decoder 206. . .

DETDESC:

DETD(238)

I/O . . . DRAM uses the degenerated address formed of column address bits different from column address bits CA<1:0>. In the fast page **mode** operation, it is possible to utilize a structure which uses the standardized degenerated address for simultaneously selecting a required number of memory cells. The fast page **mode** operation can be achieved without any problem, even if a plurality of memory cells are simultaneously selected in accordance with. . . memory cells are specified with external column addresses). However, if bits CA<1:0> are used as the counter address in the **pipeline burst mode**, it is impossible to form the semiconductor memory device with the **pipeline burst mode** and the fast page **mode** on the same semiconductor chip (because address pins are different, and pin compatibility is lost).

DETDESC:

DETD(239)

In . . . device of x4-bit and 8K-refresh type, the degenerated address applied to I/O circuits IOa-IOd is CA<10:8> in the fast page **mode** as shown in FIG. 46. Memory cells of 8 bits are simultaneously selected and are compressed into data of 1. . . of the memory cells. Meanwhile, when semiconductor memory device of x8-bit and 8K-refresh type is to be operated in the **pipeline burst mode**, the degenerated addresses must be CA<8> and CA<1:0>. The counter address outputs internal column address bits CA<1:0>. Among the memory. . .

DETDESC:

DETD(240)

As . . . selected memory block, memory cell data of 4 bits are compressed into data of 1 bit in the multibit test **mode**. In this case, the address applied to I/O circuits IOa-IOh in the fast page **mode** is CA<9:8>, and these column address bits CA<9:8> form the degenerated address. In the **pipeline burst mode**, the counter address is CA<1:0>, and the column address bits CA<1:0> form the degenerated address.

DETDESC:

DETD(241)

In . . . the semiconductor memory device, an external central processing unit (CPU) can be accessed with column address bits CA<1:0> in the **burst mode**. Also in the 64-Mbit DRAM, it is necessary to allow access with column address bits CA<1:0> in the **burst mode** (for maintaining compatibility of the semiconductor memory device). The following problem would arise if the standardized degenerated address were used as the counter address in order to accomplish both the **pipeline burst mode** and the fast page **mode** on the same semiconductor chip.

DETDESC:

DETD(242)

For . . . but different column address bits A<10:9> are to be accessed, one of the semiconductor memory devices allows access in the **burst mode** and thus allows fast access, but the other semiconductor memory device cannot make the access in the **burst mode**. Now, an arrangement will be described below with which both the fast page **mode** and the **pipeline burst mode** are accomplished on the same semiconductor chip and CA<1:0> can be used as the counter address in either **mode**.

DETDESC:

DETD(246)

Referring . . . in the case where a semiconductor memory device of x8-bit having a 8K-refresh cycle is to be operated in the **pipeline burst mode**, connection is made as follows in the semiconductor memory device having address input pins and address input pads arranged as. . .

DETDESC:

DETD(247)

In this case, the degenerated address is column address bits CA9 and CAB. The counter address in the **pipeline burst mode** is generated in accordance with the address applied to address input pads P8 and P9. Therefore, the degenerated address can. . .

DETDESC:

DETD(248)

Referring . . . case where a semiconductor memory device of a x4-bit structure having a 8K-refresh cycle is to be operated in the **pipeline burst mode**, connection is made as follows. Address input pin

terminals A0 and A1 are connected to address input pads P10 and. . .

DETDESC:

DETD(250)

FIG. . . . address input pads in a DRAM which has a x8-bit structure and a 4K-refresh cycle and can operate in the **pipeline burst mode**. Referring to FIG. 49B, address input pin terminals A0 and A1 are connected to address input pads P10 and P9,. . .

DETDESC:

DETD(251)

FIG. . . . address input pads in a 64-Mbit DRAM of a x4-bit structure which has a 8K-refresh cycle and operates in the **pipeline burst mode**. Address input pin terminals A0 and A1 are connected to address input pads P11 and P10, respectively. Address input pin. . .

DETDESC:

DETD(253)

By . . . pin terminals to the address pads internally generating the degenerated address, the DRAM which can selectively support the fast page **mode** and the **pipeline burst mode** can be formed on the same semiconductor chip.

DETDESC:

DETD(254)

In the above embodiment, the fast page **mode** has been referred as an operation **mode** in which the output high impedance state is set when column address strobe signal ZCAS is inactive, and the **pipeline burst mode** has been referred to as an operation **mode** in which the high impedance state is set only when both of column address strobe signal ZCAS and row address strobe signal ZRAS are inactive. However, the invention can be applied to operation **modes** other than the above.

DETDESC:

DETD(255)

As . . . a low current consumption, has pin compatibility with those of former generations, and can achieve either of the fast page **mode** and the **pipeline burst mode**.

9. 5,652,724, Jul. 29, 1997, Burst **EDO** memory device having pipelined output buffer; Troy A. Manning, 365/189.05, 233 [IMAGE AVAILABLE]

US PAT NO: 5,652,724 [IMAGE AVAILABLE] L2: 9 of 9
DATE FILED: Feb. 10, 1995
TITLE: Burst **EDO** memory device having pipelined output buffer

ABSTRACT:
An . . . and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a **burst** access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each **burst** access. Read/Write commands are issued once per **burst** access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a **burst** access will terminate the

burst access, reset the **burst** length counter and initialize the device for another **burst** access. A two stage **pipelined** output buffer latches read data in a first stage while data from a second stage is driven from the device.. . . is latched in the first stage. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page **Mode** and Extended Data Out Single In-Line Memory Module pinouts, and other memory circuit designs.

SUMMARY:

BSUM(5)

There . . . valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (**EDO**) mode. In an **EDO** DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held. . . output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or **EDO** DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of. . . data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the **EDO** mode, as adopted by the various DRAM manufacturers.

SUMMARY:

BSUM(11)

An . . . standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed **burst mode** of operation is provided where multiple sequential accesses occur following a single column address, and data is input and output relative to the /CAS control signal. In the **burst mode** of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read /Write commands are issued once per **burst** access eliminating the need to toggle the Read /Write control line at high speeds. Only one control line per memory. . . each /CAS typically controls only a byte width of the data bus. A data output buffer has a two stage **pipeline mode** of operation which allows for further speed increases by latching read data in an intermediate data latch, and allowing internal. . . driving the data from the part. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (**EDO**) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-**burst mode** and a high speed **burst mode** allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation with a **pipelined** data output provides for faster data access times than is possible with either fast page **mode** or **EDO** DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput.. . . from the memory. Operating frequencies significantly higher than 50 megahertz are possible with this architecture due to internal address generation, **pipelined** read circuitry, an extended valid data output period, and a single lightly loaded control signal operating at the operating frequency. . .

DETDESC:

DETD(2)

FIG. . . . a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg.times.8 burst **EDO** DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide

EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first port[redacted] of a multiplexed memory. . [redacted]

DETDESC:

DETD(3)

In . . . of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst **EDO** DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays. . . address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst **EDO** DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains. . .

DETDESC:

DETD(4)

The . . . DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing **EDO** DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column. . .

DETDESC:

DETD(8)

The memory device of FIG. 1 may include the option of switching between burst **EDO** and standard **EDO** modes of operation. In this case, the write enable signal /WE 36 may be used at the row address latch. . . low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (**EDO**) page mode cycles are selected. Both the burst and **EDO** page mode cycles allow for increased memory device operating frequencies by not requiting the data output drivers 34 to place. . . circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. For **EDO** page mode cycles, the intermediate data latch is bypassed in the output buffer circuitry and data is latched directly in. . .

DETDESC:

DETD(10)

A . . . 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard **EDO** page mode DRAM, and may be mass produced to provide the functions of both the standard **EDO** page mode and burst **EDO** DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module. . .

DETDESC:

DETD(11)

Programmability of the **burst** length, /CAS latency and address sequences may be accomplished through the use of a **mode** register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the **mode** register control the required circuits on the DRAM. **Burst** length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may. . . be provided. For a latency of 1, the intermediate data latch is bypassed. For a latency of 3, an additional **pipeline** stage may be added. It may be desirable to place this additional **pipeline** stage in

the address path, or in the read data path between the memory array and the first intermediate data latch. Other **burst** length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The. . . programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The **burst** length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed **burst mode** only, selecting between standard fast page **mode** (non-**EDO**) and **burst mode**, and using the output enable pin (/OE) 42 in combination with /RAS to select between **modes** of operation. Also, a WCBR refresh cycle could be used to select the **mode** of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional **modes** of operation such as switching between fast page **mode**, **EDO** page **mode**, static column **mode** and **burst** operation through the use of various combinations of /WE and /OE at /RAS falling time. One **mode** from a similar set of **modes** may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired **mode**. Alternately, a device with multiple **modes** of operation may have wire bond locations, or programmable fuses which may be used to program the **mode** of operation of the device.

DETDESC:

DETD(12)

A preferred embodiment of a sixteen bit wide burst **EDO** mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and. . .

DETDESC:

DETD(13)

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and **EDO** DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16. . .

DETDESC:

DETD(14)

It should be noted that the pinout for this new burst **EDO** memory device may be identical to the pinout for a standard **EDO** DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The. . . also allows for ease of new designs by those of skill in the art who are familiar with the standard **EDO** DRAM. Variations of the described invention which maintain the standard **EDO** DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device. . . disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard **EDO** pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence. . .

DETDESC:

DETD(17)

FIG. . . . in multiplexers 56 and 58. The unlatched data signals are selected for /CAS latencies equal to one, and for normal **EDO** page mode operation. For /CAS latencies greater than one, the select logic 60 will select the latched data to pass. . .

DETDESC:

DETD(20)

The . . . driver control inputs. The select logic circuit shown also has a burst mode signal BURST input for selecting between Burst **EDO** and normal **EDO** modes of operation. Pullup and pulldown signals 64 and 66 respectively from the output data latch drive the output driver. . .